What is claimed is:

1. A semiconductor integrated circuit device, comprising:

(a) a semiconductor substrate having an SiGe layer and a first Si layer epitaxially grown thereover, and having element formation regions each partitioned by element isolation regions;

(b) a shallow groove isolation which has a groove formed in each of the element isolation regions and an insulating film inside of the groove, said groove penetrating through the first Si layer and having a bottom in the SiGe layer;

(c) a second Si layer formed between the shallow groove isolation and the SiGe layer; and

(d) a semiconductor element formed over the main surface of the semiconductor substrate in the element formation regions.

2. A semiconductor integrated circuit device according to Claim 1,

wherein the element formation regions are each a region exposed from the semiconductor substrate in a semiconductor region of a first conductivity type or in a semiconductor region of a second conductivity type which is an opposite conductivity type to the first conductivity type, and

wherein the semiconductor region has a bottom in the SiGe layer.

3. A semiconductor integrated circuit device according to Claim 2, wherein the semiconductor region has a bottom at a position deeper than the bottom of the shallow groove isolation.

4. A semiconductor integrated circuit device according to Claim 1,

wherein the element formation regions are first to third element formation regions,

wherein the first and second element formation regions are exposed from the semiconductor substrate in a first semiconductor region having a first conductivity type,

wherein the third element formation region is exposed from the semiconductor substrate in a second semiconductor region having a second conductivity type which is an opposite conductivity type to the first conductivity type,

wherein a minimum width (H2) of the element isolation region between the third and the first or second element isolation regions is greater than a minimum width (H1) of the element isolation region between the first and second element formation regions, and

wherein the bottom of each of the first and second semiconductor regions exists in the SiGe layer.

5. A semiconductor integrated circuit device

according to Claim 4, wherein the bottom of each of the first and second semiconductor regions exists at a position deeper than the bottom of the shallow groove isolation.

6. A semiconductor integrated circuit device according to Claim 1, wherein the insulating film has a thermal oxide film formed over the inside wall of the groove and a second insulating film inside of the groove.

7. A semiconductor integrated circuit device according to Claim 6, wherein a nitride film is formed between the thermal oxide film and the second insulating film.

8. A semiconductor integrated circuit device according to Claim 7, wherein the nitride film is formed not over the bottom of the groove but over the side walls of the groove.

9. A semiconductor integrated circuit device according to Claim 6, wherein the second insulating film is a silicon oxide film formed by CVD using ozone and tetraethoxysilane as raw materials.

10. A semiconductor integrated circuit device according to Claim 1, wherein the second Si layer is formed to cover the shallow groove isolation.

11. A semiconductor integrated circuit device according to Claim 1, wherein the second Si layer is made of single crystal Si.

12. A semiconductor integrated circuit device according to Claim 1, wherein the second Si layer is made of polycrystalline Si.

13. A semiconductor integrated circuit device according to Claim 1, wherein the second Si layer is formed not between the shallow groove isolation and the first Si layer but between the shallow groove isolation and the SiGe layer.

14. A semiconductor integrated circuit device according to Claim 1,

wherein the semiconductor element is MISFET, said MISFET having a gate electrode formed over the semiconductor substrate via a gate insulating film, and source and drain regions formed in the semiconductor substrate on both sides of the gate electrode, and

wherein a conductive film existing as the same layer with the gate electrode is formed over the element isolation regions of the semiconductor substrate.